Simulation-based Study of Single-Event Burnout in 4H-SiC High-Voltage Vertical Superjunction DMOSFET: Physical Failure Mechanism and Robustness vs. Performance Tradeoffs

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(Dated: 13 January 2022)

We explore and elucidate the physical failure mechanisms in a 4H-SiC, high voltage, superjunction (SJ) vertical DMOSFET from a single heavy ion strike using 3-dimensional electro-thermal transient simulations. The Single-Event Burnout (SEB) failure is thermal runaway from second breakdown, initiated by impact ionization and terminated with mesoplasma formation, at the center of the P-pillar/N+ substrate interface. We also demonstrate that the SEB performance of this SiC SJ DMOSFET is insensitive to the pillar width, but sensitive to the strike location, with ion strike at the P-pillar causing SEB at a lower blocking voltage than at the N-pillar. Compared to commercially available 1.2 kV blocking-rated non-SJ DMOSFET, which has been demonstrated to survive SEB up to 525 V, the SJ DMOSFET increases SEB survival threshold voltage (V_{SEB}) by a factor of 2.2, making it close to 1200 V, while the on-resistance is increased by only 11%. Using our recently developed Figure of Merit (FoM), which considers the tradeoff between V_{SEB} and on-state performance, we find that the SiC SJ DMOSFET achieves a FoM that is 14 times better, making it superior to conventional 1.2 kV SiC DMOSFET for long-term radiation-tolerant operation in space applications.

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Vertical 4H-SiC-based high-voltage power switching devices have attracted significant interests over the last few years due to their electrical and thermal (efficiency) advantages over their silicon counterparts. However, just like silicon devices, they are prone to radiation effects and experience Single-Event Effects (SEEs) ranging from permanent increase in blocking leakage current to thermal destruction[1–4] under a single heavy ion strike, with the latter phenomenon called Single-Event Burnout (SEB). The failure mechanism for SEB has been attributed to the triggering of the parasitic NPN transistor in both Si and SiC power devices[4,5]. By contrast, we have previously identified, with 3-dimensional, physically rigorous, electro-thermal device simulations, the mesoplasma formation at the drift layer/substrate interface from second breakdown to be the primary cause of SEB failure in conventional SiC planar DMOSFETs for a timescale less than 10 nanoseconds[6,7]. However, failure mechanisms have not been identified for SEB phenomenon in SiC superjunction (SJ) devices. Would it be the same as Si SJ devices found before[5,8,9], or the same as our previous finding in conventional SiC DMOSFETs[6,7]? In this letter, we report on our study to explore and elucidate the physical failure mechanism in the SEB failure of SiC SJ MOSFETs. Also, we determine and compare the SEB performance and the static performance tradeoff with the specific on-resistance of the 4H-SiC SJ and a non-SJ conventional 1.2 kV rated DMOSFET[10] with the SEB survival threshold voltage (V_{SEB})/breakdown voltage (BV) ratio and our recently developed Figure of Merit (FoM).

V_{SEB} usually occurs at less than 50% of the rated blocking voltage for conventional vertical SiC diodes and DMOSFETs[4,11]. The SJ device structures, due to its quasi-rectangular electric field profile, has better specific on-resistance ($R_{on,sp}$) vs. blocking voltage tradeoff when compared to vertical non-SJ planar DMOSFET[12]. We are providing here a timely evaluation on the robustness of SiC SJ DMOSFETs to SEB and show its potential for long-term operations in radiation environments such as space electronics applications.

Fig. 1 shows the 3-dimensional (3D) diagram and 2-dimensional (2D) cross section of the simulated SJ DMOSFET design, using surface stripe cell geometry with a pitch of 9.5 μm. The thickness of the epitaxial drift layer is 35 μm and uses a balanced doped pillar design[13,14]. This thickness allows the breakdown voltage to be approximately 6000 V which provides sufficient overhead to survive SEB close to 1200 V. The pillar structure is orientated 90 degrees to the epitaxial/substrate surface. Four different pillar widths were investigated to determine the pillar width effect on the V_{SEB}. The basic static performance of the SJ

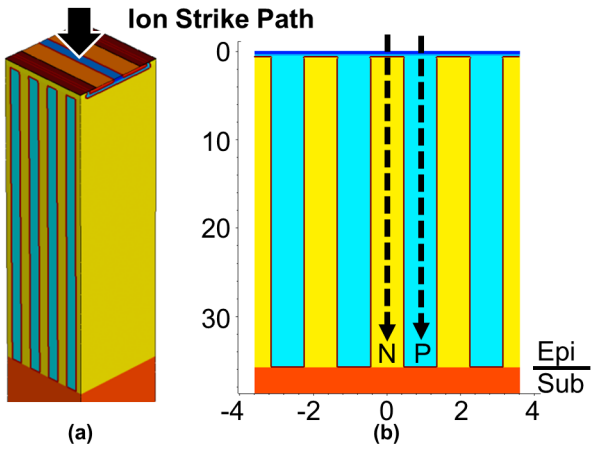

FIG. 1. SJ DMOSFET diagram showing a a) 3-D overview and a b) 2-D cross section across the pillar structure. The dashed arrows denote the heavy ion strike path. Blue is P-pillar and yellow is N-pillar. Axis in units of μm

TABLE I. Summary of static performance for SJ planar DMOSFETs

Epitaxial Doping (cm^{-3})	Pillar Width (μm)	BV (V)	$R_{on,sp}$ ($m\Omega \cdot cm^2$)
3.0x10^{16}	2.4	5957	4.8
6.0x10^{16}	1.2	5942	3.5
8.0x10^{16}	0.9	5937	3.3
1.2x10^{17}	0.6	5932	3.0

planar DMOSFET designs is summarized in Table I.

The SEB event was simulated using 3D radiation and transient electro-thermal models described in previous work[7,15–17]. Although most literature reports SEB analysis based on 2D models[18–20], a previous experimental work has demonstrated that simulations based on 2D models would lead to wrong conclusions (due to substantial underestimation of electric field)[5]. The heavy ion transport in power device was simulated by Monte Carlo transport code MCNP[17]. The ion-induced (due to ionization collisions) electron-hole (e-h) pair distributions in axial and radial directions were then used in a TCAD simulator for device response simulations. To capture the sharp variation of e-h pair distribution in space, a selective refinement scheme, where the area around and along the heavy ion track is refined

to elements sizes of 50 nm in all three dimensions, was employed. This mesh progressively becomes coarser away from the ion track and when the track enters the substrate region. Also, to capture the extreme conditions (high field up to 4.0 MV/cm and high temperature up to 3000K) that occur during an SEB event[3,6], physical parameters that govern the thermal and electrical behaviors, such as thermal conductivity, lattice heat capacity, impact ionization, and bandgap, were carefully evaluated and selected based on previous theoretical and experimental studies[21–24]. In our study, a silver ion with a Linear Energy Transfer (LET) of 46 MeV-cm^2/mg was assumed in all simulations. The selection of silver at this specific LET value is to match the experiment setup in power device radiation testing[11]. SEB was declared when the lattice temperature reaches 3000 K in simulation, which is the decomposition temperature of SiC. This simulation methodology has previously been shown to produce SEB results that agree with experimental results for non-SJ conventional 1.2 kV rated DMOSFETs[6].

In order to explore the SEB failure mechanism, the SEB performance of the SJ DMOSFETs were evaluated based on the factors of strike location and pillar width design, and the results are summarized in Table II. Three prominent phenomena are observed from simulations: (1) The failure (a mesoplasma formation) location always occurred at the interface between the pillar and substrate, independent of configurations explored, (2) the P-pillar strike location is the weakest location, with the V_{SEB} at least 100 V lower than the N-pillar strike, and (3) V_{SEB} is not affected by pillar width. To explain the above observations, we first should understand the failure mechanism in SJ DMOSFET when struck by an ion.

To explore the failure mechanisms in detail, the time evolution of electro-thermal response is examined. The SJ device with the 1.2 μm P-pillar structure is selected as a representative for the study, with the blocking voltage at 1200 V. Other structures showed similar responses. In general, it is observed that the heavy ion generates electron-hole pairs forming a microplasma along its strike path and the generation finishes by 2 ps. These generated carriers' density exceeds the background doping concentration by several orders. With such a high density, any depletion region in the device where the ion track intersects with disappears immediately (ionized donors or acceptors are neutralized by excess electrons and holes). Conduction channel (due to shorting) is established along ion track from source to drain. The carriers then traverse the epitaxial layer with the holes and electrons going towards the source and drain, respectively, and distort the electric field profile.

TABLE II. Summary of simulated SEB performance for SJ planar DMOSFETs

Pillar Width (μm)	V_{SEB} (V)		Failure Location	
	N-Pillar	P-Pillar	N-Pillar	P-Pillar
2.4	1350	1150	Pillar/ Substrate	Pillar/ Substrate
1.2	1250	1150	Pillar/ Substrate	Pillar/ Substrate
0.9	1250	1150	Pillar/ Substrate	Pillar/ Substrate
0.6	1250	1150	Pillar/ Substrate	Pillar/ Substrate

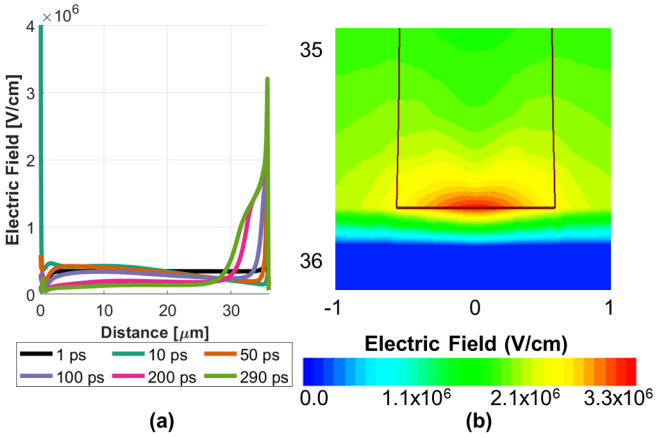

FIG. 2. Time evolution of the electric field for the 1.2 μm P-pillar at 1200 V; where a) is along the heavy ion strike path and b) is a 2-D cross-section at 290 ps after the start of the simulation. In b) both x- and y-axis are in μm and the maroon line denotes the junction

By 10 ps, the electric field is enhanced under the source contact and at the pillar/substrate interface as seen in Fig. 2a. This is due to a buildup of excess holes under the source contact and electrons at the pillar substrate interface. The enhancement under the source contact is short-lived and disappears after 50 ps, because the carriers quickly diffuse laterally and wash away the depletion regions between N+ source and P-body regions. Thus, shorting the

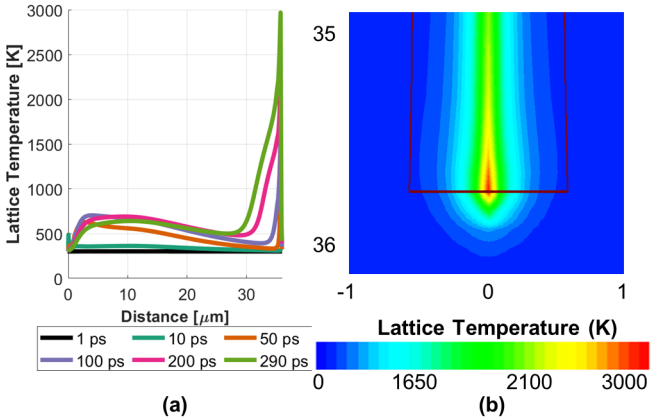

FIG. 3. Time evolution of the lattice temperature for the 1.2 μm P-pillar at 1200 V; where a) is along the heavy ion strike path and b) is a 2-D cross-section at 290 ps after the start of the simulation. In b) both x- and y-axis are in μm and the maroon line denotes the junction

source/body and body/drift junctions and causing an injection of electrons from the source region. These electrons help to balance the excess holes beneath the source contact and effectively neutralize the electric field. However, the electric field at the epitaxial/substrate interface increases and reaches 3.2 MV/cm by 50 ps and maintains this value until SEB occurs by 290 ps (Fig. 2b). Additionally, it is observed that the electric field is not only enhanced at pillar/substrate interface but also at the sidewall of the pillars adjacent to the heavy ion path due to the disruption of the space charge balance within the SJ pillars.

By 10 ps, the electric field is enhanced under the source contact and at the pillar/substrate interface as seen in Fig. 2a. This is due to a buildup of excess holes under the source contact and electrons at the pillar substrate interface. The enhancement under the source contact is short-lived and disappears after 50 ps, because the carriers short the source/body and body/drift junctions causing an injection of electrons from the source region. These electrons help to balance the excess holes and effectively neutralize the electric field. However, the electric field at the epi/substrate interface increases and reaches 3.2 MV/cm by 50 ps and maintains this value until SEB occurs by 290 ps (Fig. 2b). Additionally, it is observed that the electric field is not only enhanced at pillar/substrate interface but also at the sidewall of the pillars adjacent to the heavy ion path due to the disruption of the space charge balance within the SJ pillars.

From Fig. 2b, both electric field magnitudes, one at the sidewall and one at the pil-

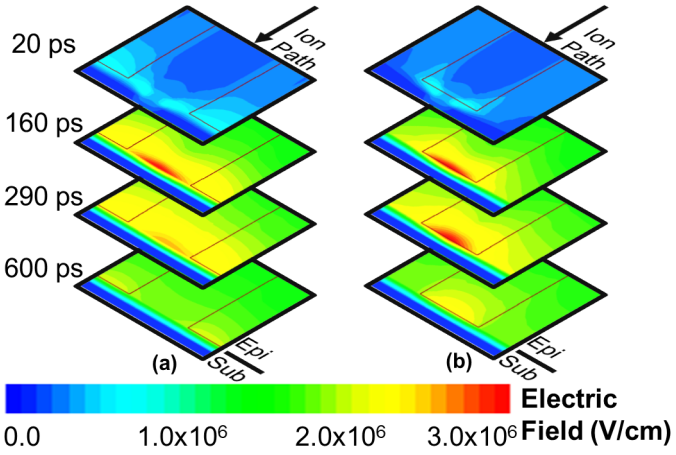

FIG. 4. 2-D time evolution of the electric field magnitude at 1100 V for a) N-pillar and b) P-pillar strikes.

lar/substrate interface, are above 2.2 MV/cm but the field at pillar/substrate interface is primarily attributed to SEB failure. This is due to the difference of the field direction at the two locations. At sidewalls, lateral fields dominate and vertical fields are almost zero. The ionization path for the charge carriers due to lateral fields is small because lateral fields change from a maximum value to zero from sidewall to the center of the pillar, thus quenching the energy of the carriers and reducing impact ionization. At pillar/substrate interface, vertical field achieves maximum at the center and maintains the maximum along the ion track, while lateral fields are almost zero. Therefore, the vertical field at the pillar/substrate interface results in a larger ionization path for the charge carriers leading to higher impact ionization rate than the lateral field at the sidewalls. The generated carriers cause an increase in the local current density at the interface, and through Joule heating, the lattice temperature increases at this location. This process continues until a mesoplasma forms, and the lattice temperature reaches 3000 K shortly after 290 ps as shown in Fig. 3. At this point the device has failed thermally and SEB is declared. There were no indications that the BJT transistor latched-up at any point during the simulation and no current flow in the device could be attributable to the transistor. Therefore, the SEB failure mechanism is from the formation of a mesoplasma due to severe impact ionization at the pillar/substrate interface causing the thermal destruction of the device.

The increased SEB sensitivity for the P-pillar strike can be explained due to the presence of the blocking P/N junction at the pillar/substrate interface. This junction, initially having

TABLE III. Summary of SEB performance and FoM for SJ and Non-SJ planar DMOSFETs

Structure	Pillar Width (μm)	V_{SEB}/BV N-Pillar	V_{SEB}/BV P-Pillar	$R_{on,sp}$ (mΩ·cm^2)	$R_{1DLimit}$ (mΩ·cm^2)	FoM P-Pillar Strike: $\frac{V_{SEB}R_{1DLimit}}{BVR_{on,sp}}$
1.2 kV non-SJ[10]	N/A	0.30		2.7	1.0	0.1
SJ	2.4	0.23	0.19	4.8	22.2	1.0
SJ	1.2	0.21	0.19	3.5	22.1	1.3
SJ	0.9	0.21	0.19	3.3	22.0	1.4
SJ	0.6	0.21	0.19	3.0	22.0	1.5

a higher electric field than the N-pillar/N+ substrate junction, can more easily reach high electric field. This is seen by examining the N-and P-pillar strikes at 1100 V, which is a common voltage where both devices survive SEB. As shown in Fig. 4, the electric field is enhanced at the pillar/substrate interface for both strikes. At 160 ps, the N-pillar electric field begins to recover while the P-pillar maintains a high value of 3.2 MV/cm until 290 ps where it begins to recover. This extended period of high electric field causes additional heating at the pillar/substrate interface that ultimately contributes to the early failure of the P-pillar strike.

As for V_{SEB} insensitivity to pillar width, this can be explained using the operation principle of SJ DMOSFETs. To create the quasi-rectangular electric field profile, the space charge needs to be balanced between the P- and N-pillars. When the heavy ion strikes the device, this space charge balance is destroyed from the resulting generated charge carriers and causes the electric field enhancement at the pillar/substrate interface. No matter how wide the pillars are made, this space charge balance is always destroyed and results in the SEB failure at the same voltage.

In order to show the performance advantage of the SJ DMOSFET, a comparison of the SJ with the non-SJ DMOSFET must be made. Table III shows the SEB performance metrics for the SJ planar DMOSFETs along with a non-SJ conventional 1.2 kV DMOSFET[10]. In general, the ratio of SEB survival threshold voltage and breakdown voltage (V_{SEB}/BV) is used to measure a device's rad-hard performance and has been widely reported in rad-hard

testing experiments[25]. However, this ratio parameter does not account for device on-state performance, leading to a biased comparison. A more complete rad-hard assurance criterion requires considerations of both on-state and rad-hard performance. For that purpose, we have introduced a FoM, as seen in Table III. This FoM accounts for both SEB robustness and on-state characteristics by normalizing the V_{SEB} to BV and the $R_{on,sp}$ to the 1-D limit ($R_{1DLimit}$) for a given BV. Since the specific on-resistance of the SJ devices can be lower than the 1-D limit[12], the SJ DMOSFET has a FoM that is 14 times better than the 1.2 kV non-SJ DMOSFET. This is due to the much lower $R_{on,sp}$ that the SJ design can achieve despite having a V_{SEB}/BV ratio that is 42% lower compared to 1.2 kV non-SJ DMOSFET. This makes the SiC SJ DMOSFET a competitive candidate for radiation hardened applications.

To summarize, we have studied the robustness of SJ SiC DMOSFETs subjected to a single heavy ion strike and explored their failure mechanisms. We demonstrated that the failure mode to be from mesoplasma formation and excessive heating at the P-pillar/substrate interface, due to the enhancement of the electric field from the electron-hole pairs generated. In addition, we have found that these SJ DMOSFETs can achieve 14 times better tradeoff between the V_{SEB} and $R_{on,sp}$ when compared to a 1.2 kV rated non-SJ DMOSFET. It should be noted that our simulation study assumes perfect crystalline structures in 4H-SiC. In reality, there are commonly observed crystalline defects, which presents a fundamental question of the potential effect on the SEB failure mechanism as well as the device robustness. Our previous research[7] indicates that unless these defects cause substantial changes of carrier saturation velocity or thermal conductivity in 4H-SiC, the effect can be small or negligible. Future research is desired to warrant more quantitative conclusions on the crystalline defect effects.

This work was supported by an Early Stage Innovations grant (NNX17AD05G) from NASA's Space Technology Research Grants Program. The first author is also supported by the Nuclear Regulatory Commission Fellowship Program under the grant 31310018M0003.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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